REMARKS/ARGUMENTS

In the Office action mailed December 18, 2003, claims 1-44 (numbered as claims 1-43) were pending in the application. The drawings were objected to, the specification was objected to, the claims were objected to due to misnumbering, one claim was rejected under 35 U.S.C. § 112, and all of the claims were rejected under either 35 U.S.C. § 102 or 35 U.S.C. § 103. Applicants thank the Examiner for attention to the application.

The specification is now amended, Figure 2 is now amended, and claims 1-3, 13, 14, 19, 23, 26, 30, 32, 36, 37, 39, and 42 are now amended, and claims 27-29, 34, 38, 41, and 44 are cancelled.

The drawings are objected to as failing to comply with 37 C.F.R. 1.84(p)(5) because reference 21 is shown on FIG. 2 but not described in the specification and reference E2 is shown on FIG. 5 but not described in the specification.

Reference numeral 21 of FIG. 2, which corresponds to the input signal equalization circuit, is already included in the specification at page 11, line 16. Thus, amendment to the specification to add the reference numeral 21 is not believed to be further required. In the specification, page 8, line 34 has been amended to include the reference numeral E2 of FIG. 5, which corresponds to the second element described in the specification.

The drawings are also objected to under 37 C.F.R. 1.83(a) because they fail to show AL2-ALN and PL2-PLN on FIG. 5 and X1 and X2 on FIG. 2. The specification is now amended with regard to the description of FIG. 5 to state what is clear from the

figure in the description, namely that a single active element and a single programmable register are illustrated for the purposes of clarity. Figure 2 is also amended to include the references X1 and X2.

The disclosure is also objected to because the acronym "PBRS is used on page 20 but not defined in the specification" (Office action, page 3). A review of the specification indicates that the acronym is PRBS. It is believed that the acronym PRBS in the relevant art is well-known to refer to pseudo-random binary sequence. In this regard, see also FIG. 1 of the "Study of LVDS Serial Links for the ATLAS Level-1 Calorimeter Trigger" cited by the Examiner. The specification is amended to explicitly indicate that the acronym PRBS refers to pseudo-random binary sequence.

The claims are objected to as two claims are numbered as claim 32. The Office action indicates that misnumbered claim 32 (second occurrence) 32-43 has been renumbered 33-44. Applicants will continue to use the numbering suggested by the Examiner in this application. Any difficulties caused by the misnumbering of claims is regretted, and Applicants thank the Examiner for attention to this detail. In addition, in submitting the additional claims (incorrectly numbered 23-43) the claim fee was inadvertently incorrect. Applicants now correct for this by submitting additional funds to correct the amount paid for additional claims.

Claim 32 was rejected under 35 U.S.C. § 112, first paragraph. Claim 32 has been amended to specify that the impedance corresponding to the first capacitance is

approximately unity at higher frequencies, as suggested in the Office action. It is respectfully submitted that omission of the term higher frequencies was an error of a typographical sort, and it was both the intention of the Applicant and the general understanding of the reader of the claims that such was inherently in the claim as originally submitted.

Claim 1, as amended specifies "a first conducting layer having a pattern forming multiple first transmission lines and a second conducting layer having a pattern forming multiple second transmission lines,...with an insulating layer separating the first conducting layer and the second conducting layer." Dayton discloses, for example, a 2X2 switch module comprising two input conductors into output conductors. Each output conductor traverses two input conductors. Dayton, col. 3, lines 21-25. In Dayton, the module shown in FIG. 2 may be implemented in a single monolithic integrated circuit chip by use of conventional photolithographic techniques. Dayton, col. 3, lines 51-53. Accordingly, it does not appear that Dayton discloses "a first conducting layer having a pattern forming multiple first transmission lines and a second conducting layer having a pattern forming multiple second transmission lines,...with an insulating layer separating the first conducting layer and the second conducting layer" as specifies by claim 1. Therefore, claim 1 is allowable in view of Dayton.

In addition, claim 1 also specifies "a semiconductor substrate with a plurality of active elements and a plurality of programmable registers corresponding to the plurality of active elements." The Office action states that Dayton teaches of

programmable registers (44) coupled to the active elements (40a-d), with the active elements coupled to one transmission line in one direction and one transmission line in the other direction. Office action, page 5. Even if Dayton discloses such, however, it does not appear that Dayton teaches placement of the active elements on a semiconductor substrate, with the transmission lines as further specified by claim 1. Accordingly, claim 1 is further allowable in view of Dayton.

Claims 1 and 2-25, depending ultimately on claim 1, are therefore allowable.

The Office action also indicates that much is understood in the art. In view of the foregoing, and later, statements it is not necessary to inquire as to whether these aspects are understood in the art. However, in the event that the rejection of claim 1, or other claims, is maintained, it is respectfully requested that evidence of what is understood in the art be provided.

Claim 26 has been amended to largely incorporate the text of claims 39 and 34. With respect to claim 34, the Office action states that Dayton teaches of a switch module and that Morgan teaches of a passive network having a predefined precompensation frequency response. The Office action, page 11. Claim 26, and substantially prior claim 34, specifies "wherein the first and second resistance, the first and second capacitance and the shunt resistance are fabricated on a monolithic integrated circuit substrate, and at least one of the first and second resistance, the first and second capacitance and the shunt resistance is one of segmented, programmable, and

a combination thereof; and wherein an impedance of the at least one of the first and second resistance, the first and second capacitance and the shunt resistance is selectable after being fabricated on the monolithic integrated circuit substrate." A review of Dayton and Morgan does not appear to disclose such. Accordingly, claim 26, and dependent claims 30-33 are allowable.

Claim 35 has been amended to substantially include the text of prior claims 41 and 44. With regard to prior claim 44, the Office action states that "Dayton, Morgan, and Huq remain silent as to having a capacitor frequency response approximately the inverse of the frequency response of the amplifier chain. Given the choice of any capacitance as described in claim 30, the system of Dayton, Morgan, and Huq would have exhibited the properties of claim 44. It would have been obvious to one skilled in the art at the time of invention to select a capacitance for a precompensation filter that would have reduced the Inter-symbol interface [sic] (ISI) including compensating for the distortion of the amplifying filters since Morgan suggests using a capacitance value to condition the incoming signal and it is well known in the art that a reduction in ISI means that faster switching can be achieved." Office action, p. 18. As an initial matter, from the references provided with the Office action it does not appear obvious to one skilled in the art at the time of the invention to select a capacitance for a precompensation filter that would have reduced ISI. Instead, it appears that merely a suggestion to condition an incoming signal is provided. In any event, however, claim 35, as amended, specifies that at least one of the two series resistors, the two

series capacitors, and the shunt resistor is one of segmented, programmable, and a combination thereof, and wherein an impedance value of the at least one of the two series resistors, and the shunt resistor is selectable after being fabricated on the circuit substrate." It does not appear that the cited references disclose such, and the Office action is silent as to these features. Accordingly, claim 35, and dependent claims 36, 37, 39, 42, and 43 are also allowable.

Accordingly the claims are now in condition for allowance and allowance of same is respectfully requested.

Respectfully submitted,
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